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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,505	04/12/2004	Han-Ping Chen	24061.226 / 2003-1180	3049
42717	7590	06/09/2006	EXAMINER	
HAYNES AND BOONE, LLP 901 MAIN STREET, SUITE 3100 DALLAS, TX 75202			LINDSAY JR, WALTER LEE	
			ART UNIT	PAPER NUMBER
			2812	
DATE MAILED: 06/09/2006				

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/822,505	Applicant(s) CHEN ET AL.	
	Examiner Walter L. Lindsay, Jr.	Art Unit 2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 15-39 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 26 and 30 is/are allowed.
- 6) ☒ Claim(s) 15, 16, 19, 22-24, 28, 31 and 34-36 is/are rejected.
- 7) ☒ Claim(s) 17, 18, 20, 21, 25, 27, 29, 32, 33 and 37-39 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |  |
|---|--|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)            |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____  |

### **DETAILED ACTION**

This Office Action is in response to an Election filed on 10/25/2005.

Currently, claims 15-39 are pending.

#### ***Specification***

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

#### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 15, 16, 19, 22-24, 28, 31, 34-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (U.S. Patent No. 6,524,915 dated 2/25/2003).

Kim shows the method as claimed in Fig. 7A-7O and corresponding text as: providing a substrate (200) having a protective layer (201) located thereon and a plurality of isolation structures (203) extending through the protective layer and at least partially into the substrate (col. 6, lines 49-59); forming a mask (205) over a first portion of a surface collectively formed by the protective layer and the plurality of isolation structures, the masked first portion thereby sharing a boundary with an unmasked

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second portion of the surface (col. 7, lines 9-20); removing sacrificial portions of the protective layer from within the unmasked second portion (col. 7, lines 21-32); removing the mask (col. 7, lines 21-32); forming a conformal layer (202) over remaining portions of the protective layer, the isolation structures, and in voids created by the removal of the sacrificial portions of the protective layer (col. 7, lines 33-45); planarizing the conformal layer such that the conformal layer, the isolation structures, and the remaining portions of the protective layer are substantially coplanar (col. 7, lines 46-53); removing the remaining portions of the protective layer (col. 8, lines 24-27); and forming transistors (224) in voids created by the removal of the remaining portions of the protective layer (col. 8, lines 28-35) (claim 15). Kim teaches that planarized portions of the conformal layer located between opposing isolation structures at least partially form a memory device (col. 8, lines 28-35) (claim 16). Kim teaches that the substrate is selected from the group consisting of: a silicon containing substrate; a silicon-on-insulator (SOI) substrate; a germanium epitaxial layer on a silicon substrate; a germanium epitaxial layer on a sapphire substrate; a silicon on nothing (SON) substrate; a plastic substrate; and a flexible substrate (col. 6, lines 49-59) (claim 19). Kim teaches that the protective layer comprises an oxygen containing layer (col. 6, lines 49-59) (claim 22). Kim teaches that the conformal layer comprises a gate electrode layer (202) (col. 6, lines 49-59) (claim 23). Kim teaches that the gate electrode layer has a thickness ranging between about 300 angstroms and about 2000 angstroms (col. 6, lines 49-59) (claim 24).

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Kim shows the method as claimed in Fig. 7A-7O and corresponding text as: providing a substrate (200) having a protective layer (201) located thereon and a plurality of isolation structures (203) extending through the protective layer and at least partially into the substrate, the substrate including at least one memory cell region and at least one periphery region (col. 6, lines 49-59); forming a mask over at least a portion of the periphery region and exposing at least a portion of the memory cell region (col. 7, 9-20); removing sacrificial portions of the protective layer from within the memory cell region (col. 7, lines 21-32); removing the mask (col. 7, lines 21-32); forming a conformal layer over remaining portions of the protective layer, the isolation structures, and in voids created by the removal of the sacrificial portions of the protective layer (col. 7, lines 33-45); planarizing the conformal layer such that the conformal layer, the isolation structures, and the remaining portions of the protective layer are substantially coplanar (col. 7, lines 46-53); removing the remaining portions of the protective layer (col. 8, lines 24-27); and forming transistors in voids created by the removal of the remaining portions of the protective layer (col. 8, lines 28-35) (claim 28). Kim teaches that the substrate is selected from the group consisting of: a silicon containing substrate; a silicon-on-insulator (SOI) substrate; a germanium epitaxial layer on a silicon substrate; a germanium epitaxial layer on a sapphire substrate; a silicon on nothing (SON) substrate; a plastic substrate; and a flexible substrate (col. 6, lines 49-59) (claim 31). Kim teaches that the protective layer comprises an oxygen containing layer (col. 6, lines 49-59) (claim 34). Kim teaches that the conformal layer comprises a gate electrode layer (202) (col. 6, lines 49-59) (claim 35). Kim teaches that the gate electrode layer

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has a thickness ranging between about 300 angstroms and about 2000 angstroms (col. 6, lines 49-59) (claim 36).

***Allowable Subject Matter***

4. Claims 17, 18, 20, 21, 25, 27, 29, 32, 33 and 37-39 have been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claims 26 and 30 are allowed.

6. The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

... wherein planarizing the conformal layer comprises planarizing by at least one of a chemical mechanical polishing (CMP) process and an etching process, as required by claim 26; and

... wherein the transistors formed in the voids include MOSFETs, as required by claim 30.

***Response to Arguments***

7. Applicant's arguments filed 4/4/2006 have been fully considered but they are not persuasive. The examiner views the second unmasked portion as being the portion of the protective layer that the applicant wishes to remove and views this as an etching step similar to that of Kim.

***Conclusion***

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Walter L. Lindsay, Jr.  
Primary Examiner  
Art Unit 2812

WLL

June 6, 2006